PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Gunnar Wetzker et al.
For	:	RECEIVER FOR RECEIVING FREQUENCY SIGNALS USING DELTA-SIGMA MODULATORS
Serial No.	:	10/564,293
Filed	:	January 10, 2006
Art Unit	:	2611
Examiner	:	Eboni N. Giles
Atty. Docket	:	NL 030813
Confirmation No.	:	6995

APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed July 1, 2009.

I. REAL PARTY IN INTEREST

The party in interest is NXP B.V., by way of an Assignment recorded at Reel 017470, frame 0701.

II. RELATED APPEALS AND INTERFERENCES

Following are identified any prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal:

NONE.

III. STATUS OF CLAIMS

Claims 1-9 and 11 are on appeal.

Claims 1-9 and 11 are pending.

No claims are allowed.

Claims 1-9 and 11 are rejected.

Claim 10 is canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The subject matter recited in independent claim 1 relates to: a receiver [Fig. 1: 1] comprising: a receiving stage [Fig. 1: 2] that receives frequency signals (Paragraph

[0046], lines 5-6); a mixing stage [Fig. 1: 3] coupled to the receiving stage [Fig. 1: 2] that generates converted frequency signals (Paragraph [0046], lines 7-9); a modulating stage [Fig. 1: 4] coupled to the mixing stage [Fig. 1: 3] that delta-sigma modulates the converted frequency signals (Paragraph [0046], lines 10-12); and a filtering stage [Fig. 1: 5] coupled to the modulating stage [Fig. 1: 4] that filters the delta-sigma modulated converted frequency signals (Paragraph [0046], lines 12-14), wherein the filtering stage [Fig. 1: 5; Fig. 5: 5] comprises a decimator [Fig. 5: 52] receiving an output signal from a time-control loop (Paragraph [0054], line 8) having a loop quantizer [Fig. 5: 23] and a loop filter [Fig. 5: 22].

The subject matter recited in independent claim 7 relates to: a system [Fig. 4: 100] comprising: a transmitter [Fig. 4: 101]; and a receiver [Fig. 4: 1] which comprises: a receiving stage [Fig. 1: 2] that receives frequency signals (Paragraph [0046], lines 5-6); a mixing stage [Fig. 1: 3] coupled to the receiving stage [Fig. 1: 2] that generates converted frequency signals (Paragraph [0046], lines 7-9); a modulating stage [Fig. 1: 4] coupled to the mixing stage [Fig. 1: 3] that delta-sigma modulates the converted frequency signals (Paragraph [0046], lines 10-12); and a filtering stage [Fig. 1: 5] coupled to the modulating stage [Fig. 1: 4] that filters the delta-sigma modulated converted frequency signals (Paragraph [0046], lines 12-14), wherein the filtering stage [Fig. 1: 5; Fig. 5: 5] comprises a decimator [Fig. 5: 52] receiving an output signal from

a time-control loop (Paragraph [0054], line 8) having a loop quantizer [Fig. 5: 23] and a loop filter [Fig. 5: 22].

The subject matter recited in independent claim 8 relates to: a modulating/filtering stage [Fig. 1: 10] for use in a receiver [Fig. 1: 1] comprising: a receiving stage that receives frequency signals (Paragraph [0046], lines 5-6); a mixing stage [Fig. 1: 3] coupled to the receiving stage [Fig. 1: 2] that generates converted frequency signals (Paragraph [0046], lines 7-9); a modulating stage [Fig. 1: 4] coupled to the mixing stage [Fig. 1: 3] that delta-sigma modulates the converted frequency signals (Paragraph [0046], lines 10-12); and a filtering stage [Fig. 1: 5] coupled to the modulating stage [Fig. 1: 4] that filters the delta-sigma modulated converted frequency signals (Paragraph [0046], lines 12-14), wherein the filtering stage [Fig. 1: 5; Fig. 5: 5] comprises a decimator [Fig. 5: 52] receiving an output signal from a time-control loop (Paragraph [0054], line 8) having a loop quantizer [Fig. 5: 23] and a loop filter [Fig. 5: 22].

The subject matter recited in independent claim 9 relates to: a method for receiving frequency signals comprising: generating converted frequency signals (Paragraph [0046], lines 7-9); delta-sigma modulating the converted frequency signals (Paragraph [0046], lines 10-12); and filtering the delta-sigma modulated converted frequency signals (Paragraph [0046], lines 12-14), wherein the filtering uses a decimator [Fig. 5: 52] receiving an output signal from a time-control loop (Paragraph

[0054], line 8) having a loop quantizer [Fig. 5: 23] and a loop filter [Fig. 5: 22].

The subject matter recited in dependent claim 11 relates to the following limitation: wherein the loop filter [Fig. 5: 22] further comprises: an adder [Fig. 5: 201]that combines a detected signal with a feedback signal, thereby producing a sum (Paragraph [0055], lines 8-9); an inverse z block [Fig. 5: 202]that receives the sum and produces the feedback signal (Paragraph [0055], lines 10-11); and a gain block [Fig. 5: 203]that processes the feedback signal to produce the output signal (Paragraph [0055], lines 12-13)that is sent to the loop quantizer [Fig. 5: 23]to control the decimator [Fig. 5: 52].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review:

A. On pages 2-6, the Office Action rejects claims 1, 2, and 5-9 under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent Application No. 2004/0057534 to Masenten et al. (hereinafter "Masenten") in view of U.S. Patent Application No. 2004/0210801 to Prasad et al. (hereinafter "Prasad").

B. On page 6, the Office Action rejects claim 3 under 35 U.S.C. § 103(a) as allegedly unpatentable over Masenten in view of Prasad, further in view of U.S. Patent No. 7,194,036 to Melanson (hereinafter "Melanson").

C. On pages 6 and 7, the Office Action rejects claim 4 under 35 U.S.C. § 103(a) as allegedly unpatentable over Masenten in view of Prasad and further in view of U.S. Patent No. 7,130,327 to Robinson et al. (hereinafter "Robinson").

D. On pages 7 and 8, the Office Action rejects claim 11 under 35 U.S.C. § 103(a) as allegedly unpatentable over Masenten in view of Prasad and further in view of U.S. Patent No. 6,225,928 to Green (hereinafter "Green").

VII. ARGUMENT

A. Rejection of Claims 1, 2, and 5-9 Under 35 U.S.C. § 103(a)

The Final Office Action dated June 5, 2009, rejects claims 1, 2, and 5-9 under 35 U.S.C. § 103(a) as allegedly unpatentable over Masenten in view of Prasad.

1. Independent Claims 1, 7, 8, and 9

Independent claim 1 recites, in part, the following subject matter: "wherein the filtering stage further comprises a decimator receiving a **feedback** signal from a **time-control loop** having a **loop quantizer** and a **loop filter**" (emphasis added). Independent claims 7-9 recite similar subject matter. Appellant respectfully submits that the references of record, alone or in combination, fail to disclose, teach, or suggest this subject matter.

On page 3, the Office Action correctly concedes that Masenten does not expressly disclose this subject matter. The Office Action then attempts to remedy this admitted

deficiency by applying the teachings of Prasad. In particular, the Office Action alleges that Prasad has a $\Delta\Sigma$ ADC. However, the Office Action fails to address the recited **time-control loop** having a **loop quantizer** and a **loop filter**.

Appellant respectfully submits that Prasad actually teaches away from the claimed subject matter. While Prasad does have a digital decimation filter [Fig. 1: 107], Prasad does not have a feedback loop from a detector going back to the decimator through a loop filter and a quantizer, as recited in independent claims 1-9. Instead, Prasad has the decimation filter [107] feed forward its signal to a LPF [108]. Thus, Prasad teaches away from the recited feedback signal.

Moreover, Prasad lacks the recited loop quantizer. A quantizer performs analog-to-digital conversion. In contrast, Prasad's feedback loop is a digital-to-analog converter [Fig. 1: DAC 106]. Thus, Prasad teaches away from the use of loop quantizer as Prasad's loop performs the opposite operation.

Prasad also lacks the recited loop filter. Prasad's feedback loop only includes a single element [Fig. 1: DAC 106]. Thus, Prasad is entirely silent regarding the use of a filter within a feedback loop in the claimed manner.

For the reasons detailed above, Appellant respectfully requests withdrawal of the rejections of claims 1, 7, 8, and 9 under 35 U.S.C. § 103(a).

2. Dependent Claims 2, 5, and 6

Claims 2, 5, and 6 depend from claim 1. Thus, claims 2, 5, and 6 are allowable for at least the reasons stated above in connection with claim 1, as well as for the separately patentable subject matter recited therein. Accordingly, Appellant respectfully requests withdrawal of the rejections of claims 2, 5, and 6 under 35 U.S.C. § 103(a).

B. Rejection of Claim 3 Under 35 U.S.C. § 103(a)

The Final Office Action dated June 5, 2009, rejects claim 3 under 35 U.S.C. § 103(a) as allegedly unpatentable over Masenten in view of Prasad, further in view of Melanson.

Melanson fails to remedy the deficiencies of Masenten in view of Prasad. Melanson does not provide a feedback signal to a decimator. Melanson also lacks a time-control loop having a loop quantizer and a loop filter.

Claim 3 depends from claim 1. Thus, claim 3 is allowable for at least the reasons stated above in connection with claim 1, as well as for the separately patentable subject matter recited therein. Accordingly, Appellant respectfully requests withdrawal of the rejections of claim 3 under 35 U.S.C. § 103(a).

C. Rejection of Claim 4 Under 35 U.S.C. § 103(a)

The Final Office Action dated June 5, 2009, rejects claim 4 under 35 U.S.C. § 103(a) as allegedly unpatentable over Masenten in view of Prasad, further in view of

Robinson.

Robinson fails to remedy the deficiencies of Masenten in view of Prasad. Robinson does not provide a feedback signal to a decimator. Robinson also lacks a time-control loop having a loop quantizer and a loop filter.

Claim 4 depends from claim 1. Thus, claim 4 is allowable for at least the reasons stated above in connection with claim 1, as well as for the separately patentable subject matter recited therein.

Accordingly, Appellant respectfully requests withdrawal of the rejections of claim 4 under 35 U.S.C. § 103(a).

D. Rejection of Claim 11 Under 35 U.S.C. § 103(a)

The Final Office Action dated June 5, 2009, rejects claim 11 under 35 U.S.C. § 103(a) as allegedly unpatentable over Masenten in view of Prasad and further in view of Green.

Dependent claim 11 recites, in part, that the loop filter comprises "an **adder** that combines an input signal with a feedback signal, thereby producing a sum; an **inverse z block** that receives the sum and produces the feedback signal; and a **gain block** that processes the feedback signal to produce an output signal that is sent to the loop quantizer" (emphasis added). Appellant respectfully submits that the references of record, alone or in combination, fail to disclose, teach, or suggest this subject matter.

On page 8, the Office Action correctly concedes that Masenten and Prasad do not expressly disclose an adder, an inverse z block, or a gain block. The Office Action then attempts to remedy the deficiencies of Masenten in view of Prasad by applying the teachings of Green. However, the Office Action fails to identify specific parts in Green as equivalent to the claimed subject matter.

On page 8, the Office Action alleges that Green produces an output signal that is sent to a loop quantizer to control a decimator. In response, Appellant respectfully submits that Green does not use a loop quantizer in the recited manner. Instead, decimation filters 208 send real and imaginary output signals 1020/1022 to power estimation circuitry 1018. See lines 43-45 of col. 13 in Green. The resulting power estimation value 1024 is then processed to produce gain control signals 1028/1032. See lines 45-50 of col. 13 in Green. Such an operation is clearly not equivalent to the claimed use of a time-control loop having a loop filter and a loop quantizer.

Moreover, Green does not disclose the recited adder, inverse z block, and gain block in the context of a loop filter. The power estimation circuitry 1018 of Green is a black box. Green is silent regarding any internal components of circuitry 1018.

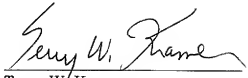
While Green may separately disclose adders and delay blocks, Green clearly does not provide a loop filter comprising an adder, inverse z block, and a gain block. Green certainly does not disclose such a loop filter sending a feedback signal to a decimator.

Accordingly, Appellant respectfully requests withdrawal of the rejections of claim 11 under 35 U.S.C. § 103(a).

CONCLUSION

For at least the reasons discussed above, it is respectfully submitted that the rejections are in error and that claims 1-9 and 11 are in condition for allowance. Therefore, Appellant respectfully requests that this Honorable Board reverse the rejections of claims 1-9 and 11.

Respectfully submitted,
KRAMER & AMADO, P.C.



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VIII. CLAIMS APPENDIX

CLAIMS INVOLVED IN THE APPEAL:

1. (Previously Presented) A receiver comprising:

a receiving stage that receives frequency signals;

a mixing stage coupled to the receiving stage that generates converted frequency signals;

a modulating stage coupled to the mixing stage that delta-sigma modulates the converted frequency signals; and

a filtering stage coupled to the modulating stage that filters the delta-sigma modulated converted frequency signals, wherein the filtering stage comprises a decimator receiving an output signal from a time-control loop having a loop quantizer and a loop filter.

2. (Previously Presented) The receiver of claim 1, wherein the modulating stage comprises:

a delta-sigma modulator comprising:

a low-pass filter;

a quantizer coupled to the low-pass filter; and

a digital-to-analog converter that feeds back an output of the quantizer to an input of the low-pass filter.

3. (Previously Presented) The receiver of claim 2, wherein the low-pass filter comprises a time-continuous filter.

4. (Previously Presented) The receiver of claim 1, further comprising:

a further mixing stage coupled to the filtering stage that generates baseband signals; and

a further filtering stage coupled to the further mixing stage that performs channel selective filtering of the baseband signals.

5. (Previously Presented) The receiver of claim 1, wherein the mixing stage comprises a mixer, and the modulating stage comprises a delta-sigma modulator.

6. (Previously Presented) The receiver of claim 1, wherein the mixing stage comprises:

a first mixer that generates in-phase signals and

a second mixer that generates quadrature signals, and

the modulating stage comprises:

a first delta-sigma modulator that delta-sigma modulates the in-phase signals, and

a second delta-sigma modulator that delta-sigma modulates the quadrature signals.

7. (Previously Presented) A system comprising:

a transmitter; and

a receiver which comprises:

a receiving stage that receives frequency signals;

a mixing stage coupled to the receiving stage that generates converted frequency signals;

a modulating stage coupled to the mixing stage that delta-sigma modulates the converted frequency signals; and

a filtering stage coupled to the modulating stage that filters the delta-sigma modulated converted frequency signals, wherein the filtering stage comprises a decimator receiving an output signal from a time-control loop having a loop quantizer and a loop filter.

8. (Previously Presented) A modulating/filtering stage for use in a receiver comprising:

a receiving stage that receives frequency signals;

a mixing stage coupled to the receiving stage that generates converted frequency signals;

a modulating stage coupled to the mixing stage that delta-sigma modulates the converted frequency signals; and

a filtering stage coupled to the modulating stage that filters the delta-sigma modulated converted frequency signals, wherein the filtering stage comprises a decimator receiving an output signal from a time-control loop having a loop quantizer and a loop filter.

9. (Previously Presented) A method for receiving frequency signals comprising:

generating converted frequency signals;

delta-sigma modulating the converted frequency signals; and

filtering the delta-sigma modulated converted frequency signals, wherein the filtering uses a decimator receiving an output signal from a time-control loop having a loop quantizer and a loop filter.

10. (Canceled)

11. (Previously Presented) The receiver of claim 1, wherein the loop filter further comprises:

an adder that combines a detected signal with a feedback signal, thereby producing a sum:

an inverse z block that receives the sum and produces the feedback signal; and

a gain block that processes the feedback signal to produce the output signal that is sent to the loop quantizer to control the decimator.

IX. EVIDENCE APPENDIX

A copy of the following evidence 1) entered by the Examiner, including a statement setting forth where in the record the evidence was entered by the Examiner, 2) relied upon by the Appellant in the appeal, and/or 3) relied upon by the Examiner as to the grounds of rejection to be reviewed on appeal, is attached:

NONE.

X. RELATED PROCEEDINGS APPENDIX

Copies of relevant decisions in prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal are attached:

NONE.